SR

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/473,868	12/28/1999	KAZUTAKA HANAOKA	0941.63502	1561

7590 09/09/2003

PATRICK G BURNS ESQ
GREER BURNS & CRAIN LTD
300 S WACKER DR SUITE 2500
CHICAGO, IL 60606

EXAMINER
ABDULSELAM, ABBAS I

ART UNIT	PAPER NUMBER
2674	18

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/473,868	HANAOKA ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (USPN 6005646) in view of Hayama et al. (USPN 5936598).

Regarding claims 1 and 8, Nakamura teaches a liquid crystal display system with a crystal layer (1) located between glass substrates (2) and (3). See Fig 3. Nakamura teaches a thin film transistor, TFT (6) in connection to a voltage application driving method. Nakamura teaches display of pixels as it relates to LCD device as well as electrodes of thin film transistors. Furthermore, Nakamura teaches source electrodes of the TFT with respect to their corresponding display electrodes, and also teaches a common electrode (22) located on the opposed substrate. Moreover, Nakamura teaches the display electrode in connection with a formation of auxiliary capacitor (10). See column 4, lines 1-17, and Fig 7. However, Nakamura does not specifically teach a common voltage which is substantially equal to a central voltage, and the production of an electric field between an auxiliary electrode and conductor pattern. Nakamura on the other hand teaches about a voltage application control method for applying a voltage to the liquid

crystal layer. Nakamura also teaches an application of a voltage to provide an effective electric field. See column 3, lines 15-20, and column 4, lines 29-39.

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to utilize Nakamura's voltage application control method and production of an electric field for the purpose of furnishing the desired level of common voltage and electric field respectively. One would have been motivated in view of Nakamura that a voltage application control method and a process of providing an effective electric field equivalently provide the desired level of common voltage substantially equal to a central voltage, and the desired level of electric field respectively.

Nakamura has been described above. However, Nakamura does not teach a data bus line on first substrate and an auxiliary capacitance such that an auxiliary capacitance formed with a data bus line and connected parallel to pixel electrode. Hayama on the other hand teaches a signal driving circuit (8), data driving circuit (14) including pixel electrode, and liquid crystal capacitance (12) along with auxiliary capacitance (11) as configured in the driving circuit of Fig. 5.

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to replace Nakamura's TFT (6) configuration of Fig. 7 by Hayama's TFT configuration (10) of Fig. 5 for the purpose of constructing liquid crystal display panel with specific arrangement of pixel electrodes (see col. 8, lines 9-20).

Regarding claims 2-5, 7, 9-12 and 15, Nakamura teaches a voltage control method for applying a voltage to the liquid crystal layer. See column 3, lines 15-20 and column 4, lines 29-39. It would have been obvious to utilize Nakamura's voltage control method to apply any desired amount of voltage. In addition, Nakamura teaches a given voltage applied to a crystal layer in comparison with a threshold voltage. See column 1, lines 55-60.

Regarding claim 6 and 13, Nakamura teaches about a smaller vertical electric field in the vicinity of the electrodes. See column 2. Lines 60-67.

Regarding claim 14, Nakamura teaches a liquid crystal layer and a transformation of its initial homogeneous state using a high a high speed. Nakamura also teaches the application time of a pulse as it relates to the speed during the transition state. See column 1, lines 5-10 and column 4, lines 48-63.

Regarding claim 16, Nakamura teaches a transition time as compared to H-com inversion and the degree of performance with respect to liquid crystals A, B, and C.

Conclusion

2. The prior art made of record and not relied upon is considered to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat No. 5,614,730 to Nakazawa

U.S. Pat No. 5,828,356 to Stroller

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Abbas abdulselam

Examiner

Art Unit 2674